

FLASH MEMORY WITH RDRAM INTERFACE

FIELD OF THE INVENTION

[01] The present invention relates generally to memory devices and in particular the present invention relates to a non-volatile flash memory interface.

BACKGROUND OF THE INVENTION

[02] A typical Flash memory comprises a memory array that includes a large number of memory cells arranged in row and column fashion. Each of the memory cells includes a floating gate field-effect transistor capable of holding a charge. The cells are usually grouped into blocks. Each of the cells within a block can be electrically programmed in a random basis by charging the floating gate. The charge can be removed from the floating gate by a block erase operation. The data in a cell is determined by the presence or absence of the charge in the floating gate.

[03] A synchronous DRAM (SDRAM) is a type of DRAM that can run at much higher clock speeds than conventional DRAM memory. SDRAM synchronizes itself with a CPU's bus and is capable of running at 100 MHZ, about three times faster than conventional FPM (Fast Page Mode) RAM, and about twice as fast EDO (Extended Data Output) DRAM and BEDO (Burst Extended Data Output) DRAM. SDRAM's can be accessed quickly, but are volatile. Many computer systems are designed to operate using SDRAM, but would benefit from non-volatile memory.

[04] Advances in DRAM interfaces has resulted in double data rate (DDR) DRAMs. These memory devices provide data communication that is synchronized to both rising and falling edges of a clock signal. While DDR DRAMs provide for fast data communications, the data is stored in a volatile manner. Likewise, Rambus memory devices, such as RDRAM, provide a packet based alternative high-speed

[14] The present invention provides a non-volatile memory device that is compatible with rambus dynamic random access memory (RDRAM). RDRAMs generally provide output data that is synchronized to both transitions of a clock signal.

[15] Referring to Figure 1, a block diagram of a flash memory according to one embodiment of the present invention is described. The memory device includes an array of non-volatile floating gate memory cells. As known to those in the art, the non-volatile memory cells store a charge on the floating gate. The floating gate charge changes the threshold voltage of the memory cell. In traditional flash memory cells, a current-sensing scheme was employed to read the memory cells. The present invention uses a voltage-sensing scheme to read the non-volatile memory cells. Possible voltage-sensing schemes are described in U.S. Patent Applications "Differential Sensing in a Memory Using Two Cycle Pre-Charge" Serial No. 09/648,706, filed 8/25/00; "Bit Line Pre-Charge in a Memory" Serial No. 09/648,701, filed 8/25/00; "Adjustable Pre-Charge in a Memory" Serial No. 09/648,722, filed 8/25/00; and "Differential Sensing in a Memory" Serial No. 09/648,723, filed 08/25/00, each incorporated herein by reference.

[16] The flash memory of the present invention can be arranged in numerous different architectures, and Figure 1 is merely a representative architecture of the present invention. Memory device 100 includes an array of non-volatile flash memory cells 102 arranged in a plurality of addressable banks. Each memory bank can contain addressable sectors of memory cells. The data stored in the memory can be accessed using externally provided location address packets received by de-multiplex circuits 104 and 106. The address packets are decoded using column and row decode circuitry 108 and 110.

[17] Write buffer 112 and de-multiplex circuit 114 are provided to write data received on DQ lines. Similarly, multiplex circuit 116 provides read data on the DQ lines. Sense amplifier circuitry 120 is used to read the data from the flash cells, and I/O gating 122 is used to communicate with the array. Sense amplifier circuitry 120 includes bit line precharge circuitry used to read the non-volatile memory cells.

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